

9/26/18

Radio Architectures

Complex baseband representation provides the theoretical basis for moving/concentrating radio functionality to baseband

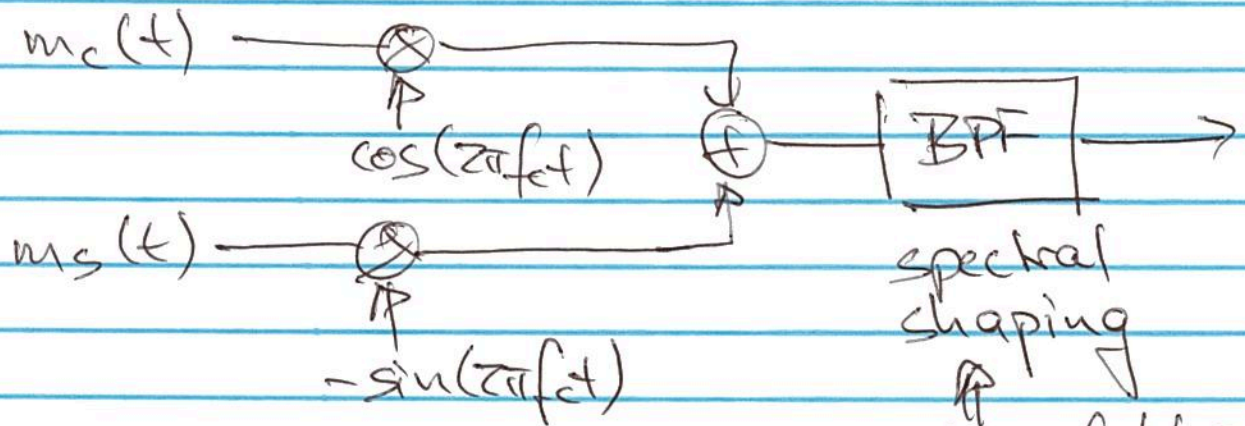
Benefits:

- Implementation is much easier at baseband
- Often/usually using digital HW

Design principle for modern radios:

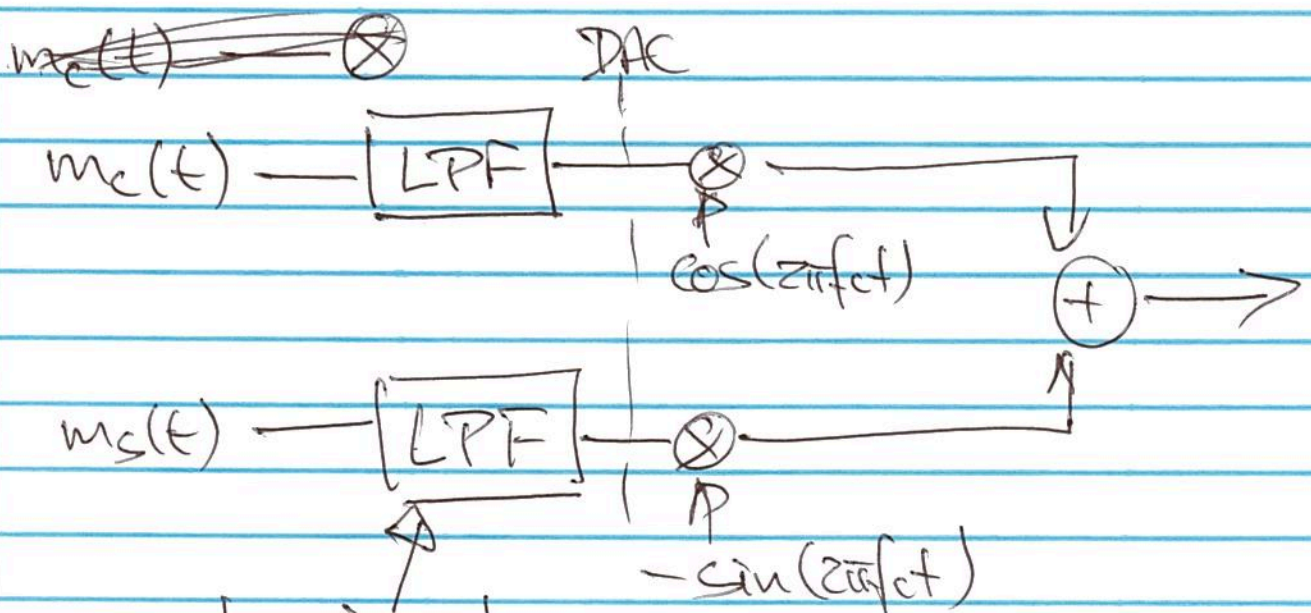
- simple analog R/F front end
- sophisticated (digital) baseband processing
- connected by AD or DA converters

Illustration: Two options for a transmitter frontend.



analog filters may be difficult if $Q = \frac{f_c}{BW}$ is large

Alternative: Filter at baseband

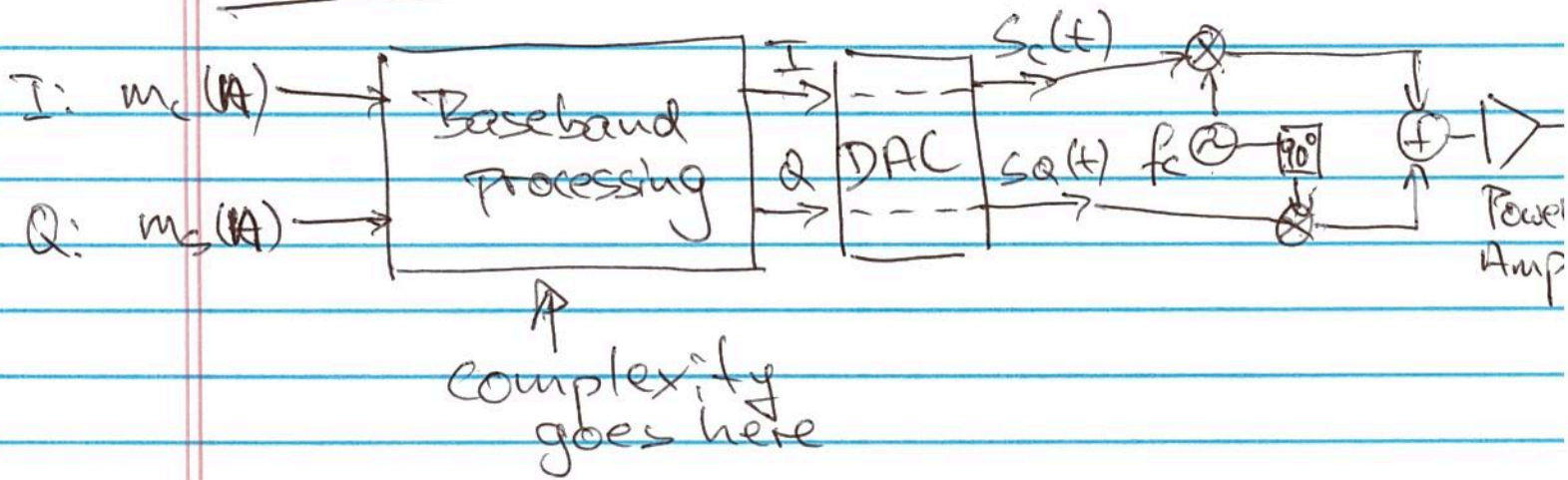


- much simpler
- may be implemented in digital HW

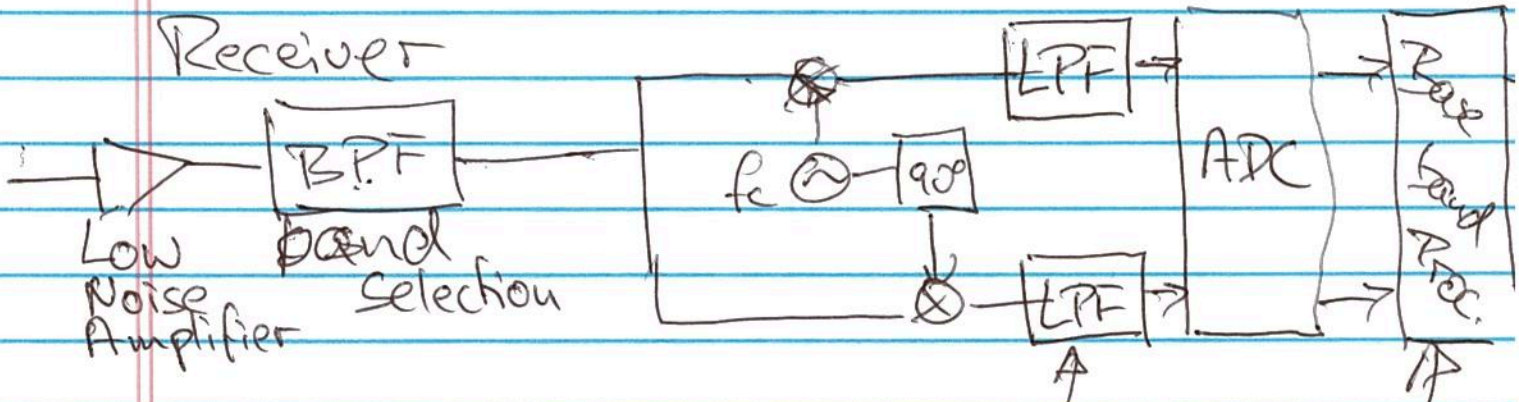
Transceiver Architectures

1. Direct conversion architecture (zero IF, homodyne)

Transmitter:



Receiver



Challenges with direct conversion:

- 1.) Amplification is easier at lower freq. - not much of an issue today
- 2.) Carrier leakage: signal from oscillator enters receiver frontend \Rightarrow DC offset.

2. Super-heterodyne Receiver Architecture

- more traditional architecture
+ avoids problems of direct conversion

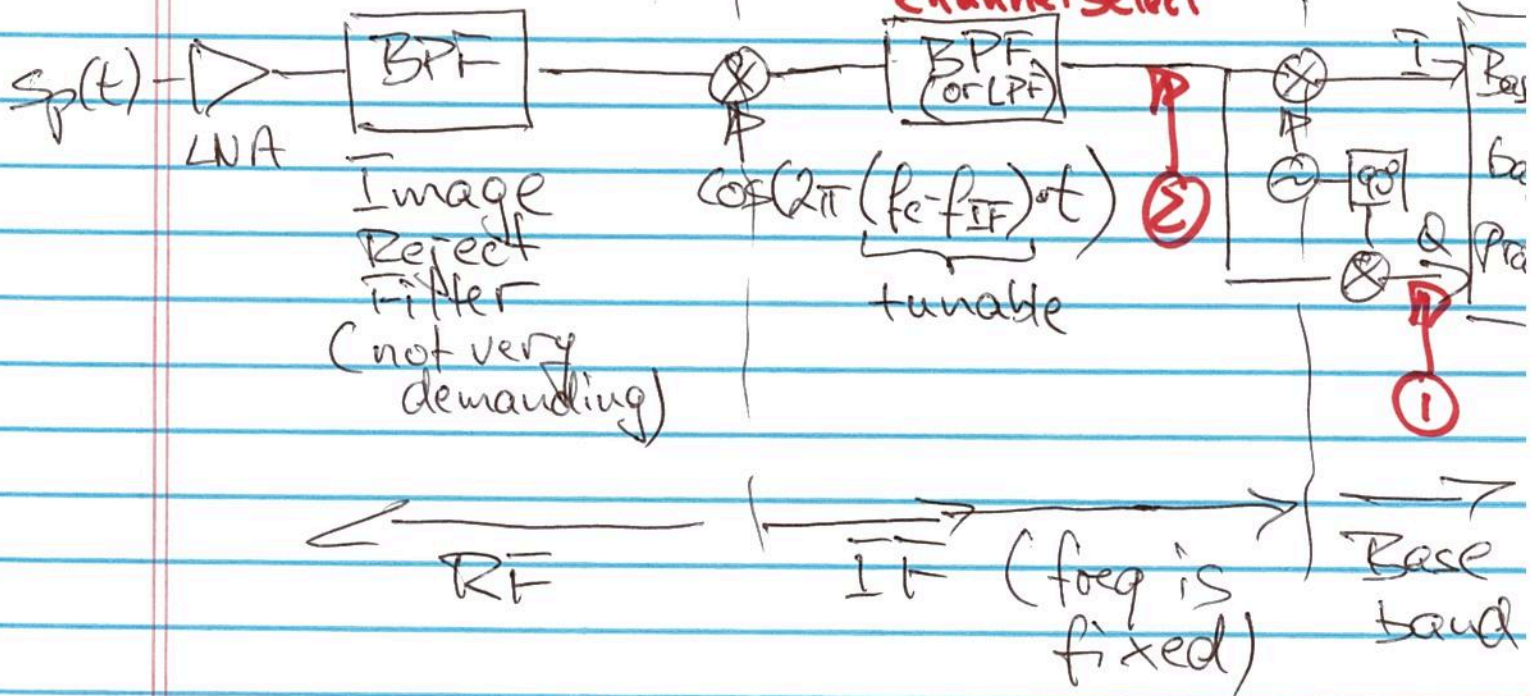
- especially carrier leakage

+ uses 2 or more step down-conversion

- From RF to IF

(intermediate freq)

- From IF to baseband

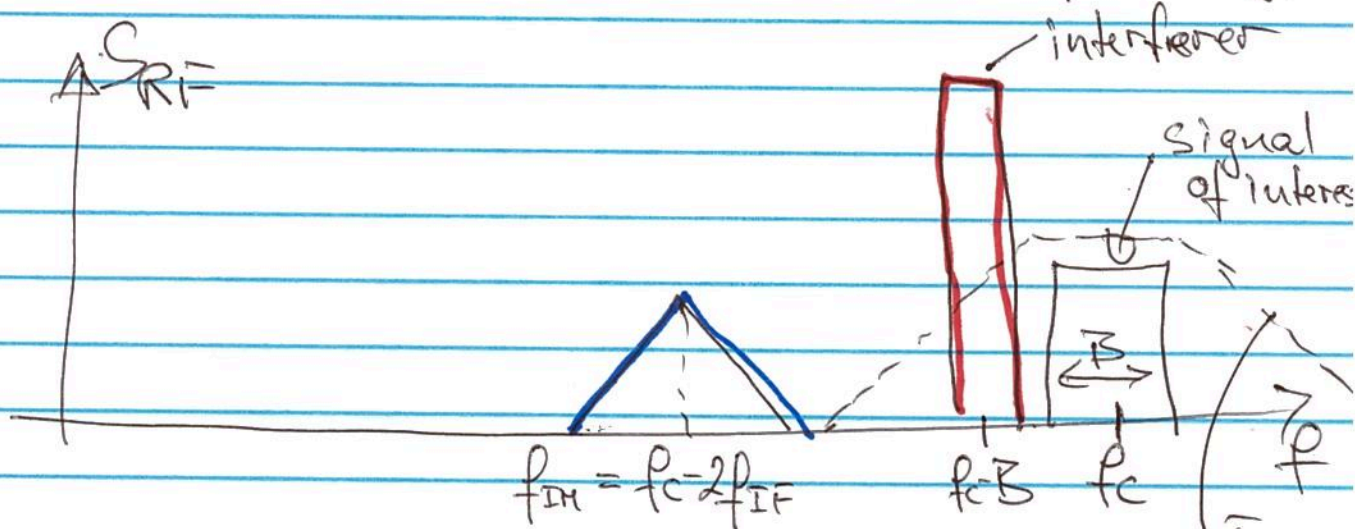


2 options for placing ADC

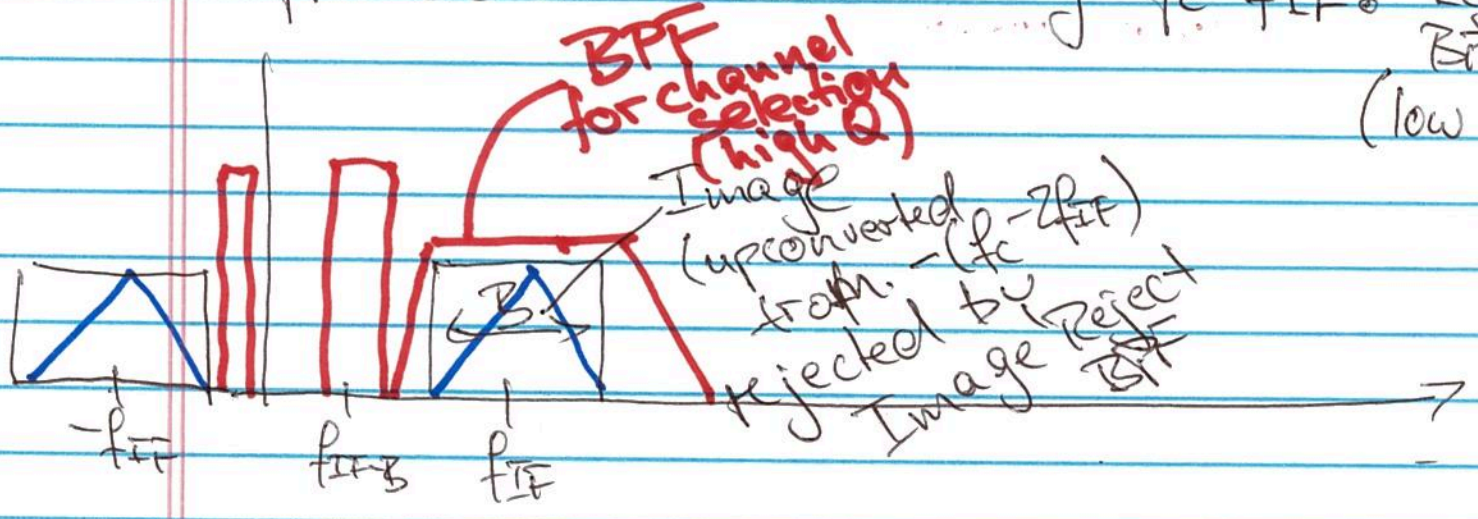
① after 2nd mixer: 2 ADCs
 $f_s \geq 2(BW)$

② after 1st mixer: 1 ADC
 $f_s \geq 1(BW)$

Spectrum of RF signal (positive freq. only)

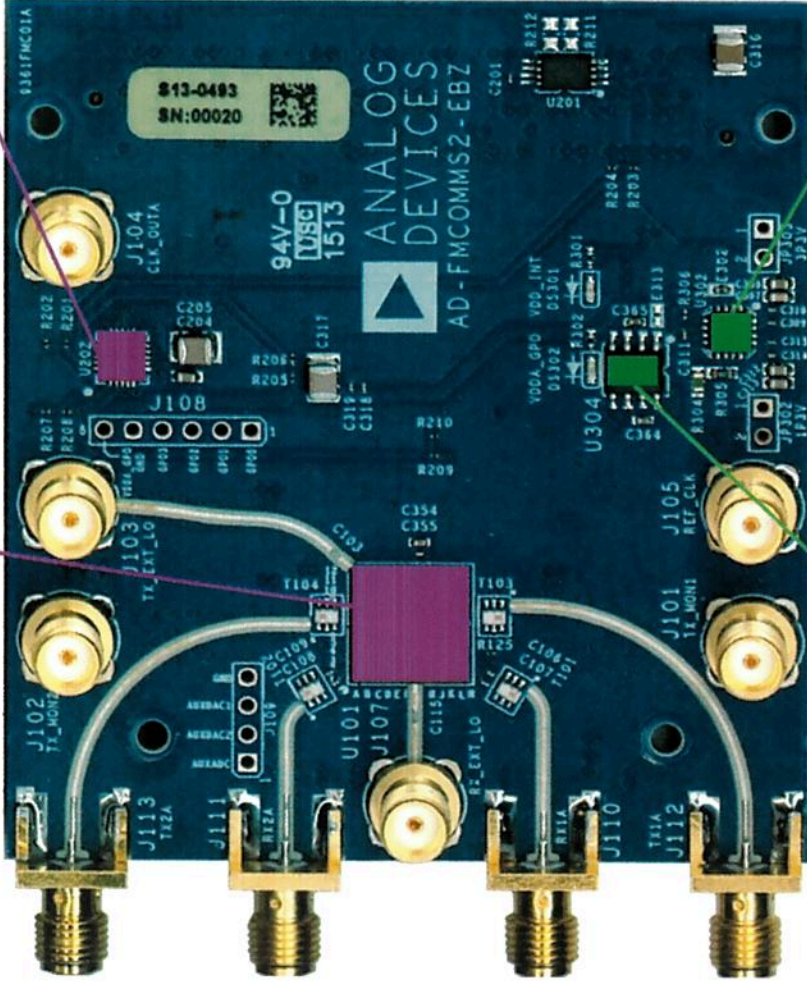


after down-conversion by $f_c - f_{IF}$:
 Image Rejected BPF (low Q)



AD9361

High performance, highly integrated RF Agile Transceiver™



ADP7104ARDZ-3.3

**High Input Voltage
500mA LDO**

ADP1755ACPZ

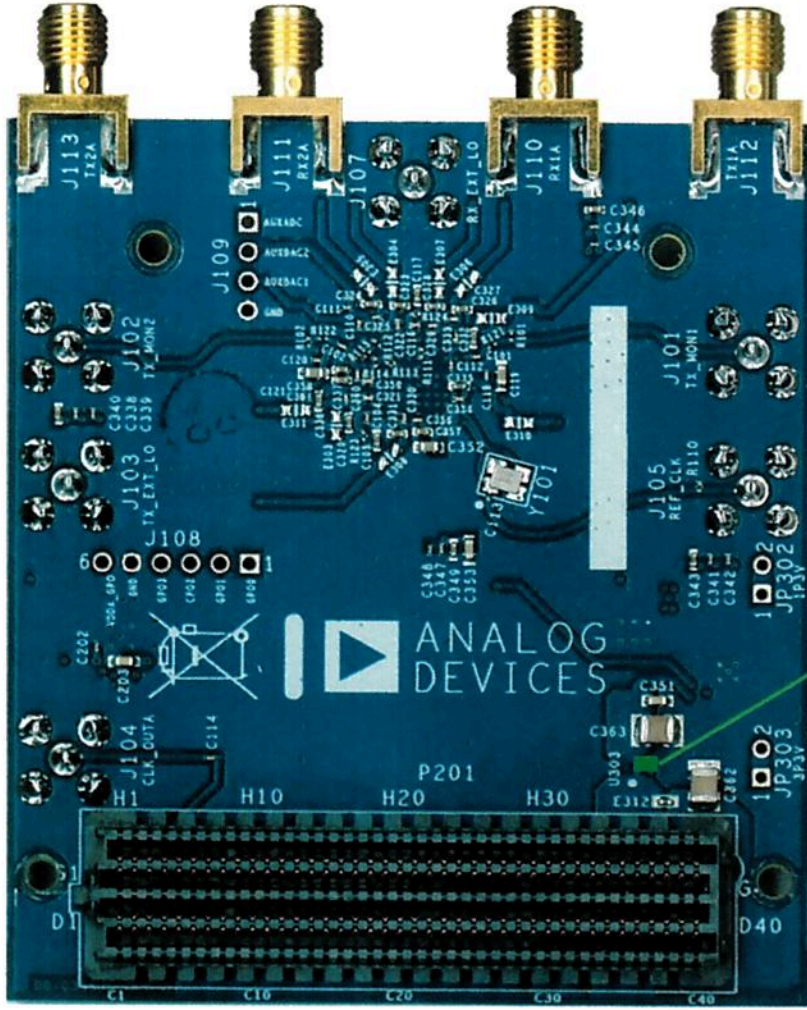
Low V_{in} / V_{out} 1.2A LDO

ADP190ACBZ

**High-side 500mA
Load Switch**

AD7291BCPZ

12-bit, low power, 8-channel, SAR ADC



FEATURES
RF 2 × 2 transceiver with integrated 12-bit DACs and ADCs
Band: 70 MHz to 6.0 GHz
Supports TDD and FDD operation
Tunable channel bandwidth: <200 kHz to 56 MHz
Dual receivers: 6 differential or 12 single-ended inputs
Superior receiver sensitivity with a noise figure of 2 dB at 800 MHz local oscillator (LO)
RX gain control

Real-time monitor and control signals for manual gain

Independent automatic gain control

Dual transmitters: 4 differential outputs
Highly linear broadband transmitter
TX EVM: ≤ -40 dB
TX noise: ≤ -157 dBm/Hz noise floor
TX monitor: ≥ 66 dB dynamic range with 1 dB accuracy
Integrated fractional-N synthesizers
2.4 Hz maximum LO step size
Multichip synchronization
CMOS/LVDS digital interface
APPLICATIONS
Point to point communication systems
Femtocell/picocell/microcell base stations
General-purpose radio systems
GENERAL DESCRIPTION

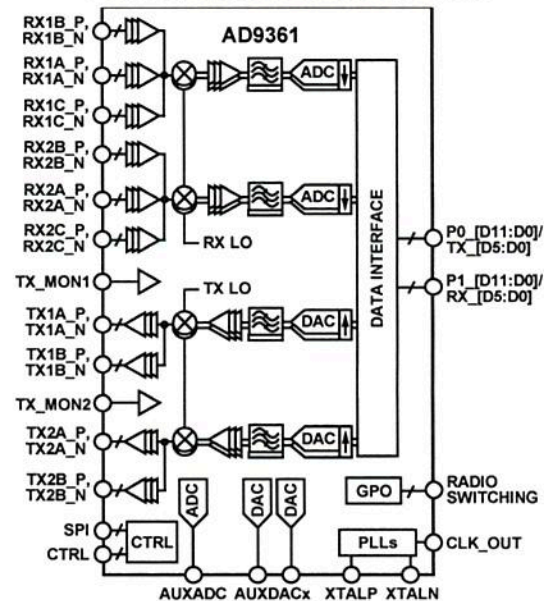
The **AD9361** is a high performance, highly integrated radio frequency (RF) Agile Transceiver™ designed for use in 3G and 4G base station applications. Its programmability and wideband capability make it ideal for a broad range of transceiver applications. The device combines a RF front end with a flexible mixed-signal baseband section and integrated frequency synthesizers, simplifying design-in by providing a configurable digital interface to a processor. The **AD9361** operates in the 70 MHz to 6.0 GHz range, covering most licensed and unlicensed bands. Channel bandwidths from less than 200 kHz to 56 MHz are supported.

The two independent direct conversion receivers have state-of-the-art noise figure and linearity. Each receive (RX) subsystem includes independent automatic gain control (AGC), dc offset correction, quadrature correction, and digital filtering, thereby eliminating the need for these functions in the digital baseband. The **AD9361** also has flexible manual gain modes that can be externally controlled. Two high dynamic range ADCs per channel digitize the received I and Q signals and pass them through configurable decimation filters and 128-tap finite impulse response (FIR) filters to produce a 12-bit output signal at the appropriate sample rate.

Rev. E

Document Feedback

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FUNCTIONAL BLOCK DIAGRAM

NOTES

1. SPI, CTRL, P0_[D11:D0]/TX_[D5:D0], P1_[D11:D0]/RX_[D5:D0], AND RADIO SWITCHING CONTAIN MULTIPLE PINS.

Figure 1.

10483-001

The transmitters use a direct conversion architecture that achieves high modulation accuracy with ultralow noise. This transmitter design produces a best in class TX EVM of < -40 dB, allowing significant system margin for the external PA selection. The on-board transmit (TX) power monitor can be used as a power detector, enabling highly accurate TX power measurements.

The fully integrated phase-locked loops (PLLs) provide low power fractional-N frequency synthesis for all receive and transmit channels. Channel isolation, demanded by frequency division duplex (FDD) systems, is integrated into the design. All VCO and loop filter components are integrated.

The core of the **AD9361** can be powered directly from a 1.3 V regulator. The IC is controlled via a standard 4-wire serial port and four real-time I/O control pins. Comprehensive power-down modes are included to minimize power consumption during normal use. The **AD9361** is packaged in a 10 mm × 10 mm, 144-ball chip scale package ball grid array (CSP_BGA).